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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Application of :
Jun OSANAI :
Serial No. 10/647,945 : Group Art Unit - 2829
Filed: August 26, 2003 : Examiner - Scott B. Geyer
For: MANUFACTURING METHOD FOR :
BIPOLAR GATE CMOS SEMI- :
CONDUCTOR DEVICE (As :
Amended) : Docket No. S004-5106

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MS NON-FEE AMENDMENT
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

S I R:

In response to the Office Action mailed September 9, 2004, applicant amends his application as follows:

ADDITIONAL FEES:

No additional fee is believed required in connection with this response. However, should it be determined that a fee is due, authorization is hereby given to charge any such fee to our Deposit Account No. 01-0268.

MAILING CERTIFICATE ON PAGE 8

IN THE TITLE:

**Kindly delete the title currently of record and
insert therefor the following new title:**

**MANUFACTURING METHOD FOR BIPOLAR GATE CMOS
SEMICONDUCTOR DEVICE**